REMARKS

Claims 11-44 are pending. Claims 11, 17, 22, 23, 26, 29, 30, 33, 34, and 40 have been amended.

Claims 11-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 4,677,737 to Corrie et al. Reconsideration of this rejection respectfully is requested.

Claim 11 recites, *inter alia*, a semiconductor device comprising "a substrate" and "at least two non-overlapping gate structures," "wherein at least one of the gate structures is a transistor gate. Corrie et al. does not disclose transistor gate structures. Indeed, the Office Action indicates on page 5 as follows: "No prior art discloses that claimed invention where the gate structures are transistor gates with or without lightly doped regions therebetween." Claim 11 and dependent claims 12 and 13 are patentable over Corrie et al.

The Office Action objects to claims 14-25 as being dependent on rejected claim 11. Independent claim 11 is patentable over Corrie et al., so dependent claims 14-25 are patentable over Corrie et al.

Claim 26 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Corrie et al. in view of U.S. Pat. No. 5,576,763 to Ackland et al. Reconsideration of this rejection respectfully is requested.

Claim 26 recites, *inter alia*, a semiconductor device comprising "a substrate," "a plurality of non-overlapping conductive transistor gates formed over the substrate," and "a lightly doped region in the substrate between two adjacent ones of the plurality of conductive gates," "wherein at least one of the two adjacent ones of the plurality of gates is a transistor gate." Corrie et al. does not disclose or suggest a semiconductor device having a plurality of "non-overlapping conductive gates," "a lightly doped region in the substrate

between two adjacent ones of the plurality of conductive gates," "wherein at least one of the two adjacent ones of the plurality of gates is a transistor gate." As noted above, the Office Action indicates on page 5 that "[N]o prior art discloses that claimed invention where the gate structures are transistor gates with or without lightly doped regions therebetween."

Ackland et al does not cure the deficiencies of Corrie et al. Ackland et al. has been cited as providing the recited lightly-doped regions that the Office Action admits are missing from Corrie et al. Applicant notes, however, that doping of the substrate takes place in Corrie et al. prior to formation of the gate electrodes. The gate electrodes are separated by dielectric. Further doping of the substrate to provide lightly-doped regions would serve no purpose in Corrie et al. Neither Corrie et al. nor Ackland et al. provide any motivation or reason for modifying Corrie et al. according to Ackland et al. as proposed in the Office Action. It appears that the only motivation for selectively modifying Corrie et al. to include lightly doped regions comes from an improper attempt at hindsight reconstruction of the present invention. Claim 26 is patentable over Corrie et al. in view of Ackland et al.

The Office Action objects to claims 27 and 28 as depending on rejected claim 26, but indicates that claims 27 and 28 contain allowable subject matter. Independent claim 26 is patentable over Corrie et al. in view of Ackland et al. As a result, dependent claims 27 and 28 are patentable over Corrie et al. in view of Ackland et al.

Claims 34-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Corrie et al. in view of Ackland et al. Claim 34 recites, *inter alia*, an image processing apparatus having an image sensor comprising "a substrate" and "at least two non-overlapping gate structures formed in a single layer on said substrate," wherein "at least one of the gates structures is a transistor gate." Corrie et al. does not teach or suggest an image processing apparatus having an image sensor featuring "at least two non-overlapping gate structures formed in a single layer on said substrate," wherein "at least one of the

gates structures is a transistor gate." The Office Action admits on page 5 that "[N]o prior art discloses that claimed invention where the gate structures are transistor gates with or without lightly doped regions therebetween."

Ackland et al. does not cure the deficiencies of Corrie et al. The Office Action states that it "would have been obvious to a person of ordinary skill in the art to form the image sensor and image processor of Ackland et al. with the gate structures of Corrie et al." Applicant respectfully disagrees. Ackland et al. discloses CMOS active pixels that include transistors, such as a reset transistor, a voltage-follower transistor, and a select transistor. Corrie et al. discloses gate electrodes, not transistor gates, which are formed as part of integrated CCDs. Moreover, the gate electrodes disclosed by Corrie et al. are formed by a complex process. There is no teaching in the prior art as to how the gate electrodes of Corrie et al. would be substituted for the transistor gates of Ackland et al. Further, neither Ackland et al. nor Corrie et al. provides the motivation necessary to modify Ackland et al. to utilize the gate electrodes of Corrie et al. Claim 34 and dependent claims 35-38 are patentable over Corrie et al. in view of Ackland et al.

Claims 40-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Corrie et al. in view of Ackland et al. Claim 40 recites, *inter alia*, a processing system having an image sensor comprising "a substrate" and "at least two non-overlapping gate structures formed in a single layer on said substrate," wherein "at least one of the gate structures is a transistor gate." Corrie et al. does not teach or suggest transistor gate structures. The Office Action indicates on page 5 as follows: "No prior art discloses that claimed invention where the gate structures are transistor gates with or without lightly doped regions therebetween."

Ackland et al. does not cure the deficiencies of Corrie et al. The Office Action states that it "would have been obvious to a person of ordinary skill in the art to form the image sensor and image processor of Ackland et al. with the gate structures of Corrie et al." Applicant respectfully disagrees. As noted above, Ackland et al. discloses CMOS

active pixels that include transistors, such as a reset transistor, a voltage-follower transistor, and a select transistor. Corrie et al. discloses gate electrodes, not transistor gates, which are formed as part of integrated CCD's. Moreover, the gate electrodes disclosed by Corrie et al. are formed by a complex, multi-step process. There is no teaching in the prior art as to how the gate electrodes of Corrie et al. would be substituted for the transistor gates of Ackland et al. Further, neither Ackland et al. nor Corrie et al. provides the motivation necessary to modify Ackland et al. to utilize the gate electrodes of Corrie et al. Claim 40 and dependent claims 41-43 are patentable over Corrie et al. in view of Ackland et al.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: July 21, 2005

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Peter McGee
Registration No.: 35,947
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant